IN THE SPECIFICATION:

(1) The paragraph [0048] at page 13 has been amended as follows:

[0048] The first blanking electrode 24 deflects the electron beam so that the electron beam may not hit the block of the mask 30. It is preferable that the first blanking electrode 24 deflects the electron beam so that the electron beam may not hit the mask 30. Since the pattern ~~generated~~ formed in the mask 30 deteriorates by the irradiation of the electron beam, the first blanking electrode 24 deflects the electron beam when the pattern is not formed on the wafer 64, so that the deterioration of the mask 30 is prevented. The focal point adjustment lens system 114 includes a third electron lens 28 and a fourth electron lens 32. The electron beam is focused on the wafer 64 by the third electron lens 28 and the fourth electron lens 32. The wafer projection system 116 includes a fifth electron lens 40, a sixth electron lens 46, a seventh electron lens 50, an eighth electron lens 52, a ninth electron lens 66, a fourth deflector 34, a fifth deflector 38, a sixth deflector 42, a main deflector 56, a sub deflector 58, a second blanking electrode 36, and a round aperture section 48.

(2) The paragraph [0049] at page 14 has been amended as follows:

[0049] The pattern image is rotated due to influence of an electric field and/or a magnetic field. The fifth electron lens 40 adjusts rotation of the pattern image of the electron beam which has passed through the predetermined opening pattern of the mask 30. The sixth electron lens 46 and the seventh electron lens 50 adjust the reduction ratio of the pattern image formed on the wafer 64 with respect to the pattern formed on the mask 30. The eighth electron lens 52 and the ninth electron lens 66 function as objective lenses. The fourth deflector 34 and the sixth deflector 42 deflect the electron beam to the direction of the optical axis A at a downstream of the mask 30 in the discharging direction of the electron beam. The fifth deflector 38 deflects the electron beam to a direction substantially parallel with the optical axis A. The main deflector 56 and the sub deflector 58 deflect the electron beam so that the electron beam is projected on the predetermined area of the wafer 64. In the present embodiment, the main deflector 56 is used for deflecting the electron beam in a subfield including a plurality of areas which can be irradiated by single shot of the electron beam (to be referred to as shot area hereinafter), and the sub deflector 58 is used for the deflection between the shot areas in the subfield.

(3) The paragraph [0051] at page 15 has been amended as follows:

[0051] The control system 140 includes a common processing section 200, ~~an~~ individual processing sections 300a and 300b, and individual control sections 120a and 120b. The individual control sections 120a and 120b include a deflection control section 82, a mask stage control section 84, a blanking-electrode control section 86, an electron lens control section 88, a reflected electron processing section 90, and a wafer stage control section 92. The common processing section 200 supplies exposure data stored in the hard disk to the individual processing sections 300a and 300b. The individual processing sections 300a and 300b supply the control data about exposure processing to each of the control sections of the individual control sections 120a and 120b based on the exposure data supplied from the common processing section 200. The deflection control section 82 controls the first deflector 18, the second deflector 22, the third deflector 26, the fourth deflector 34, the fifth deflector 38, the sixth deflector 42, the main deflector 56, and the sub deflector 58. The mask stage control section 84 controls the mask stage drive section 68, and moves the mask stage 72.

(4) The paragraph [0052] from page 15 to page 16 has been amended as follows:

[0052] The blanking electrode control section 86 controls the first blanking electrode 24 and the second blanking electrode 36. In the present embodiment, it is preferable

that the first blanking electrode 24 and the second blanking electrode 36 are controlled so that the electron beam is to be projected on the wafer 64 at the period of the exposure processing, and the electron beam is not projected on the wafer 64 ~~expect~~ except the period of the exposure processing. The electron lens control section 88 controls electric power supplied to the first electron lens 14, the second electron lens 20, the third electron lens 28, the fourth electron lens 32, the fifth electron lens 40, the sixth electron lens 46, the seventh electron lens 50, the eighth electron lens 52, and the ninth electron lens 66. The reflected electron processing section 90 detects digital data indicating the amount of electrons based on an electrical signal detected by the reflected electron detector 60. The wafer stage control section 92 moves the wafer stage 62 to a predetermined position using the wafer stage drive section 70.

(5) The paragraph [0069] from page 23 to page 24 has been amended as follows:

[0069] Next, in a development step, the exposed wafer is dipped in developer, is developed, and excessive resist is removed (S16). Then, in an etching step, the silicon substrate, insulator layer, or electric conduction film, which is in the area where the photoresist on the wafer is removed, is etched by anisotropic etching using plasma (S18). Then, in an ion implantation step, impurity, such as boron and arsenic,

is ~~poured into~~ doped in the wafer to form semiconductor devices, such as transistors and diodes (S20). Then, in an annealing step, the wafer is annealed and the ~~poured~~ doped impurity is activated (S22). Then, in a rinsing step, the wafer is rinsed with chemical to remove the organic contamination and/or metal contamination on the wafer (S24). Then, in a film deposition step, a conductive layer or an insulator layer is deposited, and a wiring layer and an insulating layer between the wirings are formed (S26). The semiconductor device, which includes an isolation area, an element area, and a wiring layer on the wafer, is manufactured by combining and repeating steps from the photoresist coating step (S12) to the film deposition step (S26). Then, in an assembly step, the wafer, in which a predetermined circuit is formed, is sliced, and the chip is assembled (S28). The semiconductor device manufacturing flow ~~is halted~~ ends in S30.

(6) The paragraph [0093] from page 32 to page 33 has been amended as follows:

[0093] Moreover, the buffer memory (PA) 310' receives the second main address from the address counter 304', outputs a second pattern starting address and second quantity information, which are examples of the exposure data, and supplies them to the address counter 306'. Then, the address counter 306' outputs a second pattern address based on the second pattern starting address and the second quantity

information, and supplies it to the buffer memory (PD) 312'. The expect memory control section 328' causes the comparing section 334' to read the ~~second~~ first pattern address from the expect memory 322' while the buffer memory (PA) 310' is outputting the second pattern starting address and the second quantity information, i.e., while the address counter 306' is outputting the second pattern address.

(7) The paragraph [0099] at page 35 has been amended as follows:

[0099] Moreover, the buffer memory (PA) 310' receives the third main address from the address counter 304', outputs a third pattern starting address and third quantity information, which are examples of the exposure data, and supplies them to the address counter 306'. Then, the address counter 306' outputs the ~~first~~ third pattern address based on the ~~first~~ third pattern starting address and the ~~first~~ third quantity information, and supplies it to the buffer memory (PD) 312'. The expect memory control section 328' causes the comparing section 334' to read a ~~third~~ first pattern address from the expect memory 322' while the buffer memory (PA) 310' is outputting the ~~second~~ third pattern starting address and the ~~second~~ third quantity information, i.e., while the address counter 306' is outputting the third pattern address.

(8) The paragraph [0136] at page 48 has been amended as follows:

[00136] Referring to Figures 6 and 7, operation of the common processing section 160' shown in Figure 10, especially a pattern error detection method, will be explained specifically hereinafter. First, the integrated control section 300' generates ~~a~~ first main expect data, which is the expected values of the first main data to be output from the buffer memory (main) 308' based on the first main address, which is an example of the control signal for exposing the band area in the frame area 202a' shown in Figure 6, and supplies it to the expect memory 320'. Then, the expect memory 320' stores the first main expect data generated by the integrated control section 300'.

(8) The paragraph [0137] from page 48 to page 49 has been amended as follows:

[00137] Moreover, the integrated control section 300' generates ~~a~~ first pattern address expect data, which is the expected values of the first pattern address to be output from the address counter 306' based on the first main address, and supplies it to the expect memory 322'. Then, the expect memory 322' stores the first pattern address expect data generated by the integrated control section 300'. Moreover, the integrated control section 300' generates ~~a~~ first pattern expect data, which is the expected values of the first pattern data to be output from the buffer memory (PD) 312' based on the first pattern address, and supplies it to the expect

memory 324'. Then, the expect memory 324' stores the first pattern expect data generated by the integrated control section 300'.

(9) The paragraph [0146] from page 51 to page 52 has been amended as follows:

[00146] Before the second exposure processing, the integrated control section 300'generates: ~~a~~ fourth main expect data, which is an expected value of fourth main data to be output from the buffer memory (main) 308' based on the fourth main address which is an example of the control signal for exposing the band area in the frame area 202b' shown in Figure 6; ~~a~~ fourth pattern address expect data, which is an expected value of a fourth pattern address to be output from the address counter 306' based on the fourth main address; and ~~a~~ fourth pattern expect data, which is the expected values of fourth pattern data to be output from the buffer memory (PD) 312' based on the fourth pattern address. Then, between the first exposure processing and the second exposure processing, the fourth main expect data is supplied to the expect memory 320', the fourth pattern address expect data is supplied to the expect memory 322', and the fourth pattern expect data is supplied to the expect memory 324'. Then, between the first exposure processing and the second exposure processing, the expect memories 320', 322', and 324' read the fourth main expect data, the fourth pattern address expect data, and the

fourth pattern expect data generated by the integrated control section 300', respectively. Then, the exposure processing of the frame area 202b' is started.

(10) The paragraph [0168] at page 59 has been amended as follows:

[00168] Before the end of the second exposure processing, the integrated control section 300' generates: ~~a~~ fifth main expect data, which is an expected value of fifth main data to be output from the buffer memory (main) 308' based on a fifth main address which is an example of the control signal for exposing the band area in the frame area 202c' shown in Figure 6; ~~a~~ fifth pattern address expect data, which is an expected value of a fifth pattern address to be output from the address counter 306' based on the fifth main address; and ~~a~~ fifth pattern expect data, which is the expected values of fifth pattern data to be output from the buffer memory (PD) 312' based on the fifth pattern address. Then, during the second exposure processing, the fifth main expect data is supplied to the expect memory 320', the fifth pattern address expect data is supplied to the expect memory 322', and the fifth pattern expect data is supplied to the expect memory 324'. Then, during the second exposure processing, the expect memories 320', 322', and 324' read the fifth main expect data, the fifth pattern address expect data, and the fifth pattern

expect data generated by the integrated control section 300', respectively.